AMENDMENTS TO THE CLAIMS

Please replace the claims, including all prior versions, with the listing of claims below.

Listing of Claims:

1. (Currently amended) A memory chip ~~having~~ comprising a substrate ~~(1)~~, into which memory cells are introduced,
the memory cells having a trench capacitor ~~(2)~~ and a transistor,
the trench capacitor at least partially having a filling ~~(3, 4)~~, and
the transistor ~~(22, 21, 28)~~ having a source terminal, ~~and~~ a drain terminal ~~(21, 22)~~ and a gate terminal ~~(28)~~,
the drain terminal ~~(21)~~ being electrically conductively connected to the trench capacitor ~~(3, 4)~~,
~~characterized in that~~wherein
the filling ~~(3, 4)~~ at least partially has a material which is unstable at high temperatures~~, in particular at temperatures of above 800°C~~, which occur during a high-temperature process ~~in the~~during fabrication of the memory chip, ~~in that~~ the filling ~~(3, 4) was~~being introduced ~~only~~ after the high-temperature processes, and ~~in that~~ the filling ~~(2, 3) was~~ not exposed to a high-temperature process.

2. (Currently amended) The memory chip as claimed in claim 1, ~~characterized in that~~wherein the filling has at least one of the materials from the following group: hafnium oxide, zirconium oxide, lanthanum oxide, yttrium oxide, and strontium titanium oxide.

3. (Currently amended) The memory chip as claimed in claim 2, ~~characterized in that~~wherein the filling has a silicate compound.

4. (Currently amended) The memory chip as claimed in claim 1, ~~characterized in that~~wherein the filling ~~(3, 4)~~ at least partially has a metallic material.

5. (Currently amended) The memory chip as claimed in ~~one of claims 1 to 4, characterized in that~~claim 1, wherein ~~the~~ a wall of the trench ~~(2)~~ is at least partially covered with a dielectric layer ~~(3)~~,

~~in that~~ a metallic layer ~~(4)~~ is at least partially applied on the dielectric layer ~~(3)~~,
~~in that~~ the metallic layer ~~(4)~~ is electrically conductively connected to the drain terminal ~~(21)~~ of the transistor via a strap filling ~~(17)~~.

6. (Currently amended) The memory chip as claimed in ~~one of claims 1 to 5, characterized in that~~claim 1, wherein an electrically conductive layer ~~(5)~~ is formed in a manner adjoining the trench ~~(2)~~ in the substrate ~~(1)~~.

7. (Currently amended) The memory chip as claimed in ~~one of claims 1 to 6, characterized in that~~claim 1, wherein the trench is covered by an epitaxial layer ~~(6)~~,
~~in that~~ an opening is introduced in the epitaxial layer ~~(6)~~,
~~in that~~ a conductive connection between the filling ~~(3, 4)~~ and the drain terminal ~~(21)~~ is formed through the opening,
~~in that~~ a dielectric layer ~~(3)~~ is at least partially applied on ~~that~~a side of the epitaxial layer ~~(6)~~ which faces the trench ~~(2)~~.

8. (Currently amended) A method for fabricating a memory cell having a trench capacitor, ~~having the following method steps of~~comprising:
_____introducing a trench ~~(2)~~ into a substrate ~~(1)~~;
_____filling the trench ~~(2)~~ at least partially with a dummy filling ~~(32)~~;
_____applying a covering layer ~~(6)~~ to the substrate ~~(1)~~, which covering layer is ~~preferably~~ formed as an epitaxial layer;
_____introducing a transistor ~~(21, 22)~~ into the covering layer ~~(6)~~;
_____removing the dummy filling ~~(32)~~ from the trench ~~(2)~~;
_____introducing a storage dielectric ~~(3)~~ and a trench electrode ~~(4)~~ into the trench ~~(2)~~, a trench capacitor being created, and
_____forming a connection of the trench electrode ~~(4)~~ to a terminal ~~(21)~~ of the transistor.

9. (Currently amended) The method as claimed in claim 8, ~~characterized in that~~wherein a channel ~~(24, 57)~~ is etched into the covering layer ~~(6)~~ as far as the dummy filling ~~(32)~~,

~~in that~~ the dummy filling ~~(32)~~ is etched out via the channel ~~(24, 47, 57)~~,
~~in that~~ a dielectric layer ~~(3)~~ is at least partially applied to the wall of the trench ~~(2)~~,
~~in that~~ a conductive layer ~~(4)~~ is applied to the dielectric layer ~~(3)~~, and
~~in that~~ the conductive layer ~~(4)~~ is electrically conductively connected to a terminal ~~(21)~~ of the transistor.

10. (Currently amended) The method as claimed in ~~either of claims 8 and 9, characterized in that~~claim 8, wherein, after the etching of the channel ~~(47, 57)~~, ~~the~~ sidewalls of the channel ~~(47, 57)~~ are covered with a protective layer ~~(62, 71), preferably~~ made of nitride, and
~~in that~~ the dummy filling ~~(32)~~ is subsequently etched out from the trench ~~(2, 3)~~.